Sub B10

WHAT IS CLAIMED IS:

1. A MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said body region;

a gate electrode disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode; and

a source electrode disposed atop said first surface and connected to each of said source regions;

said gate electrode being comprised of P-type polysilicon.

2. The MOS gated device of claim 1 in which said gate electrode is insulated from said channel region by a gate dielectric layer comprised of silicon dioxide.

Sub C2

3. The MOS gated device of claim 2 wherein said gate dielectric has a thickness of between 500 to 1000Å.

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4. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about 5.5E13.

5. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about 8.0E13.

SUB F1 cont.

6. The MOS gated device of claim 1 wherein said substrate includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip and that is less heavily doped than said chip.

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7. The MOS gated device of claim 1 wherein said base region includes a portion adjacent to said upper surface that is more heavily doped than another portion of said base region that is adjacent to a lower boundary between said base region and said substrate.

8. The MOS gated device of claim 1 further comprising an interlayer dielectric layer formed atop said gate electrode and having openings therein in which said source electrode contacts said source regions.

Sub E2

9. The MOS gated device of claim 8 wherein said interlayer dielectric is low temperature oxide.

10. The MOS gated device of claim 8 wherein said interlayer dielectric includes dopant ions.

SUB F1 cont.

11. The MOS gated device of claim 1 further comprising a passivation layer formed atop said source electrode.

12. The MOS gated device of claim 11 wherein said passivation layer is comprised of low temperature oxide.

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13. The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about 5E15.

14. A process for the manufacture of a power MOSFET having improved total dose radiation resistance

and resistance to single event failure, said method comprising the steps of:

introducing N-type dopants into an upper surface of a P-type substrate of a semiconductor wafer to form a plurality of spaced, N-type body regions;

introducing P-type dopants into said upper surface and within each of said body regions to form respective source regions, a periphery of each of said source regions being spaced from a periphery of its corresponding body region at said upper surface to define N-type channel regions therebetween;

forming a polysilicon gate electrode atop and insulated from said channel region;

introducing P-type dopants into said polysilicon gate electrode; and

forming a source electrode atop of and connected to said source regions.

15. The process of claim 14 further comprising the step of forming a gate oxide layer atop said channel regions prior to forming said polysilicon gate electrode.

16. The process of claim 15 wherein said gate oxide is formed by a pyrogenic process.

17. The process of claim 15 which further includes the step of annealing said gate oxide after the formation thereof.

18. The process of claim 14 wherein said N-type channel regions are formed by an approximately 100 KeV phosphorus implant at a dose of about 5.5E13.

19. The process of claim 14 wherein said N-type channel regions are formed by an approximately 100 KeV phosphorus implant at a dose of about 8.0E13.

20. The process of claim 15 wherein said gate oxide has a thickness of about 500-1000Å.

21. The process of claim 14 further comprising the step of forming an interlayer dielectric atop said gate electrode prior to forming said source electrode.

22. The process of claim 21 further comprising the step of forming openings to said source region and said body region in said interlayer dielectric.

23. The process of claim 22 further comprising the step of introducing dopants into said interlayer dielectric prior to forming said openings therein so that said openings have a tapered profile.

24. The process of claim 14 further comprising the step of forming a passivation layer atop said source electrode.

25. The process of claim 24 wherein said passivation layer is LTO.

26. The process of claim 14 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant having a dose of about 5E15.

27. The process of claim 14 further comprising the steps of forming an oxide layer atop said P-type substrate and patterning and etching away portions of said oxide layer prior to introducing said N-type dopants.

28. The process of claim 27 further comprising the steps of patterning and removing further portions of said oxide layer and then introducing P-type enhancement dopants into said substrate.

29. The process of claim 28 further comprising the steps of forming a further oxide layer atop said substrate, patterning and etching away portions of said

further oxide layer to form openings therein and then introducing further N-type dopants into said openings in said further oxide layer so that said base region includes a portion adjacent to said upper surface that is more heavily doped than another portion of said base region that is adjacent to a lower boundary between said base region and said substrate.

30. The process of claim 29 wherein said step of introducing P-type dopants includes introducing said P-type dopants into said openings in said further oxide layer.

31. The process of claim 14 further comprising the step of depositing a backside metal layer to a bottom surface of said silicon substrate.